

# Low-Level Test of the New Read-Out-Driver (ROD) Module and Back-of-Crate (BOC) Module for ATLAS IBL Data Acquisition System Upgrade

Bagus Hanindhito

*Department of Electrical Engineering, School of Electrical Engineering and Informatics  
Institut Teknologi Bandung, Indonesia  
Email : hanindhito@bagus.my.id*

**Abstract**—During first long shutdown of The Large Hadron Collider, most of experiment infrastructures at CERN will be upgraded for preparation to operate at higher energy thus can open new possibilities to discover the unknown in particle physics. ATLAS, which is the biggest particle detector at CERN, will also be upgraded by constructing new pixel sensor layer. This new pixel sensor layer is called ATLAS Insertable B-Layer (IBL). IBL will be installed between the existing pixel sensor and new, smaller radius beam pipe. The installation of IBL will introduce new level of radiation and pixel occupancy. Therefore, it requires development of new technologies to supports the ATLAS IBL upgrade and also improve the physics performance of the existing pixel sensor. One of the important key technologies that must be upgraded is data acquisition system. The development of new front-end ASIC, the FE-I4, to answer the challenge in data acquisition system will require new off-detector electronics. The new off-detector electronics was implemented by using two VME-based boards, the Back-of-Crate (BOC) modules which handles optical input-output functionality and the Read-Out-Driver (ROD) modules which handles data processing. By the beginning of 2014 summer, the new ROD and BOC modules will mark new milestone in production process. Both of them will undergo series of stress tests to make sure its functionality and reliability. Therefore, the systematic and comprehensive low-level tests method must be developed to test the ROD, BOC, and anything in between in an efficient and effective way. By analyzing the result of this low-level tests, improvement and revision to ROD and BOC modules both in hardware level and in firmware level can be made. Moreover, the development of current test method promises the possibilities for the future test system integration by which the end-user can test the ROD and BOC functionality without any hassle.

**Index Terms**— ATLAS Insertable B-Layer, Back-of-Crate Module, Data Acquisition System, Low-Level Test, Read-Out-Driver Module.

## I. INTRODUCTION

SINCE its first physics run in 2009, Large Hadron Collider (LHC), the world's largest and most powerful particle collider built by the European Organization for Nuclear Research (CERN), has provided physicists around the world with a huge quantity of experiment data to be analyzed. LHC has opened new windows of possibilities to discover the unknown in particle physics. One of the most remarkable

discovery is the existence of Higgs particle which is confirmed by the data from LHC in 2013. After roughly four years of physics run, the LHC entered the first long shutdown, LS1, which begun on February 14, 2013. Although there will be no collisions during this two-years long shutdown, the LHC as well as others experiment infrastructures at CERN will be upgraded. This upgrade during the first long shutdown is intended to prepare the LHC and others supporting infrastructure to be taken to new level of higher maximum energy and luminosity physics run which is predicted to be 13TeV or almost twice its current maximum energy.

During this first long shutdown, some of particle detectors are also get upgraded. ATLAS detector which is the biggest particle detector at CERN is among of the detector that will be upgraded. The ATLAS detector is a general purpose detector at LHC. This toroid-shape LHC apparatus will get upgrade by installing new pixel sensor layer which is called Insertable B-Layer (IBL). This new pixel sensor layer will be installed between the existing pixel sensor and new, smaller radius beam-pipe. The installation of IBL will improve the performance of particle sensor at ATLAS without removing the old pixel sensor layer.

On the other hand, the installation of IBL introduces new level of radiation and pixel occupancy. Therefore, it requires the development of new technologies to supports the IBL pixel sensor layer installation. New front-end application-specific integrated circuit (ASIC) has been developed as an answer to the challenge of data acquisition to keep up with the new requirement of pixel sensor layer. The FE-I4 ASIC, the successor of FE-I3 ASIC, requires new off-detector electronics to handle the data acquisition and data processing.

The new off-detector electronics are implemented by using a pair of two modules, the Read-Out-Driver (ROD) Modules and the Back-of-Crate (BOC) Modules. The two modules will be paired back-to-back by using Versa Module Europa (VME) which is as the same as the previous version. The ROD Modules will mostly handle the data processing while the BOC Modules will mostly handle the optical input/output functionality. Both ROD and BOC will have some field-programmable gate arrays (FPGA) ICs to implement its logic circuit and soft processors in which a data acquisition and processing software can be ran. Therefore, both ROD and BOC will require robust electronics circuitry as well as reliable firmware to be ready to use.

At the beginning of 2014 summer, the BOC modules and ROD modules will undergo some series of extensive test to ensure their reliability and readiness to be used as data acquisition system for ATLAS IBL upgrade. This kind of stress-test should be done comprehensively, not only for each modules but also the interconnection between modules must be tested. By analyzing the test result, improvement and revision can be made both of hardware design and firmware design so that the BOC and ROD can meet specific requirements.

There will be some various tests with different purposes. These test can be time consuming and uphill tasks to be done. Moreover, there will be more ROD and BOC coming to CERN to be tested. The development of effective and efficient test method is needed to test the functionality of ROD and BOC comprehensively.

This report mainly discuss about how the various test are done to BOC and ROD and what the results are. Moreover, this report also gives a preliminary review of the possible automatic test development that integrate all of tests by which the end user can conduct various test easily without changing the configuration.

## II. THE ATLAS INSERTABLE B-LAYER

The ATLAS Insertable B-Layer (ATLAS IBL) is the fourth layer which is added to the present pixel sensor between a new beam pipe and the current inner pixel sensor layer, the B-Layer [1]. It consists of 14 tilted staves which has 64cm long, 2cm wide, and tilted in  $14^\circ$  angles. Each staves will be equipped by 32 FE-I4 ASICs as front-end chip and its corresponding sensor.

The IBL pixel sensor layer will give ATLAS detectors capabilities and better vertexing because it is installed close to interaction point. Besides, the IBL pixel sensor layer will have

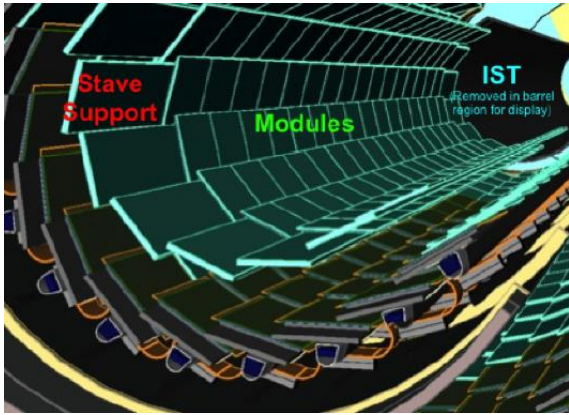


Fig. 1. The structure and arrangement of staves and IBL modules as well as the stave support in ATLAS Insertable B-Layer. [2]

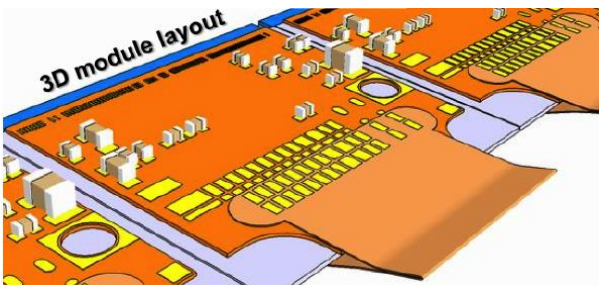


Fig. 2. Three dimensional of IBL modules. [2]

ability to compensate for module failures and to provide additional redundancy against fake combination of hits [3]. The IBL will operate until the third long shutdown, LS3, which is scheduled to be in 2022 at peak luminosity  $2 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$  at radius of 3.3cm [3].

## III. THE FE-I4 FRONT-END ASIC

The FE-I4 application-specific integrated circuit (ASIC) is the successor of FE-I3 which was used as front-end IC at ATLAS experiments. FE-I4 is designed with a 130nm CMOS process technology which gives the FE-I4 an ability to withstand higher radiation level compared to its predecessor. Moreover, the FE-I4 can also handle higher hit rate. Therefore, FE-I4 can answer the need of new data acquisition technologies for the new high luminosity LHC upgrades.

### A. Limitation of the Previous Front-End ASIC

The predecessor of FE-I4, the FE-I3, has known limitation that make the FE-I3 cannot be used for future experiments. Some of the limitation are its radiation hardness and its capability to handle high hit rates. Therefore, the FE-I3 must be replaced with the new ASIC that can be used for future experiments after LHC first long-shutdown upgrade.

### B. Design and Development the FE-I4 ASIC

The development of the FE-I4 ASIC is the answer for the need of new front-end chips which fulfill the requirements that cannot be achieved by using the old front-end. As the successor of FE-I3 ASIC, the FE-I4 has a lot of new features compared to the FE-I3. Moreover, some of FE-I3 features are also inherited to the FE-I4. In the term of size, the FE-I4 has considerably larger size compared to the FE-I3. The FE-I4 has a dimension of 20.22mm by 18.8mm whereas the FE-I3 has a dimension of 7.6mm by 11.1mm [2].

The new features of FE-I4 ASIC are listed below [5].

- PLL Clock multiplier to support high speed output from 40MHz beam clock.
- V/2 charge pump DC-DC converter without hardwired.
- The ability for the radiation detector to automatically disable the chip.
- Two triggers mode, continuous (single time slice) and stop (all time slice).
- Programmable Read Only Memory in the form of e-fuse.
- Opposite-corner alignment marks for flip-chip pattern recognition.
- Isolated sensor connection through a chip bonding pad.
- Internal error logging counters.

On the other hand, the FE-I4 features that are inherited from FE-I3 are listed below [5].

- Internal and external pulse calibration charge injection.
- Internal generation of all bias voltages and currents.
- Programmable global and pixel register with Single-Event-Upset (SEU) tolerance.
- Global discriminator OR output ("hit bus").
- Self-triggered operation mode based on hit bus.
- Analog test outputs for one or more pixels.
- Voltage regulators which is compatible with serial power.

### C. The FE-I4 Chip Layout and Block Diagram

The FE-I4 has the chip layout as depicted in figure 3 [5]. The pixel array has bump bond pads with  $12\mu\text{m}$  width on a  $50\mu\text{m}$  vertical pitch. In the horizontal direction, there is one single column of bump pads along the left and right edges, with 39 pairs of columns in between. There are  $500\mu\text{m}$  pair-to-pair spaces with  $50\mu\text{m}$  space within each pair. There also a stand-alone linear-shunt voltage regulator.

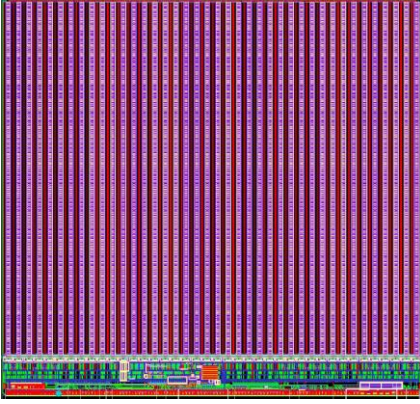


Fig. 3. FE-I4 chip layout. The FE-I4 chip layout is considerably larger than its predecessor, the FE-I3 chip. It has 20.22mm by 18.8mm dimension [5].

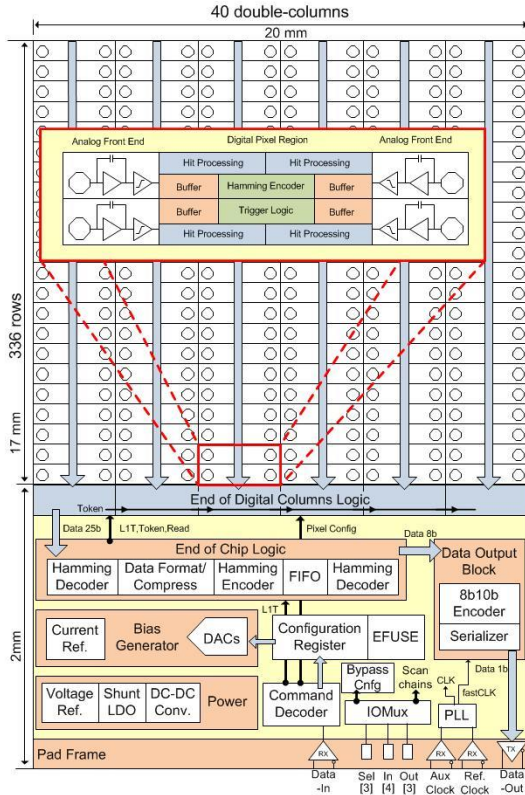


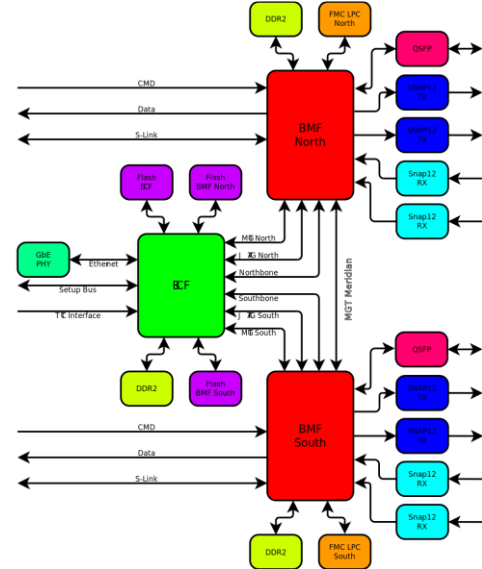
Fig. 4. FE-I4 chip block diagram. This figure also shows the digital pixel region (digital double column) that stand on two of analog columns. [5]

The FE-I4 pixel array is organized in column pairs numbered from 0 (the leftmost) until 39 (the rightmost). A column pair consists of two analog columns which have 336 pixels tall on either side of a digital double column [5]. The digital double column (digital pixel region) is actually a single column of 4-pixel regions but it is called double column because it stand on two columns of analog pixels [5].

### IV. THE ATLAS IBL BACK-OF-CRATE MODULE

ATLAS IBL Back-of-Crate (BOC) modules are responsible for handling the control interface to the detector and the data interface from the detector [6]. Both interface run via optical communication system with different speed and protocol. For the data input to the BOC, each of FE-I4 front-end chip has its own line to the BOC whereas for the data output from the BOC, each module consist of two FE-I4 front-end chips has one line to the BOC. In other words, the number of output lines is only half of the number of input lines. The BOC also handles the interface to the TTC timing system which provides 40MHz experiment clock [6]. The TTC clock is then distributed across every BOC card via the VME backplane. This clock is used as primary reference for the BOC and the ROD. The ROD itself will copy this clock to be used by itself although there is a clock generator integrated in ROD (depends on configuration).

The block diagram of the ATLAS IBL BOC is shown in figure 5. The major components for ATLAS IBL BOC is the Field Programmable Gate Array (FPGA). There are two Xilinx Spartan-6LX150T FPGA which implement the functionality of two identical BMF slices [6]. There is also one smaller FPGA (Xilinx Spartan-6LX75T) which implements the primary board-control function, the BMC.





## V. THE ATLAS IBL READ-OUT-DRIVER MODULE

The ATLAS IBL Read-Out-Driver (ROD) module is one of the components that is used in the new ATLAS data acquisition system to support the installation of new IBL pixel sensor layer. Each IBL ROD has its pair with one ATLAS IBL Back-of-Crate (BOC) module [7]. One Timing Interface Module (TIM) distributes the global timing and trigger information to the 15 IBL ROD modules. The IBL ROD modules communicate with other modules using VME and Ethernet connection.

One basic function of the IBL ROD is to transmit control commands and configuration data through IBL BOC to the FE-I4 front-end chips. Moreover, the IBL ROD also handles the received data streams from the FE-I4 front-end chips after IBL BOC performs the 8B/10B decoding. There are four Field-Programmable Gate Array (FPGAs) and one Digital Signal Processor (DSP) which responsible to operate IBL ROD functions.

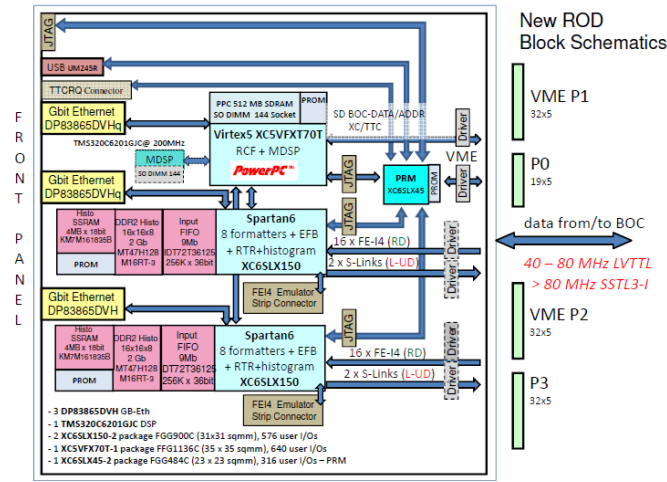


Fig. 7. ATLAS IBL ROD block schematics. Two Xilinx Spartan6 FPGAs are being used to implement two identical Slaves, the North Slave and the South Slave whereas more powerful Xilinx Virtex5 FPGA is being used as master and implements ROD control system as well as PowerPC processor. Another small Spartan6 FPGA is used to implement the program reset manager. [8]

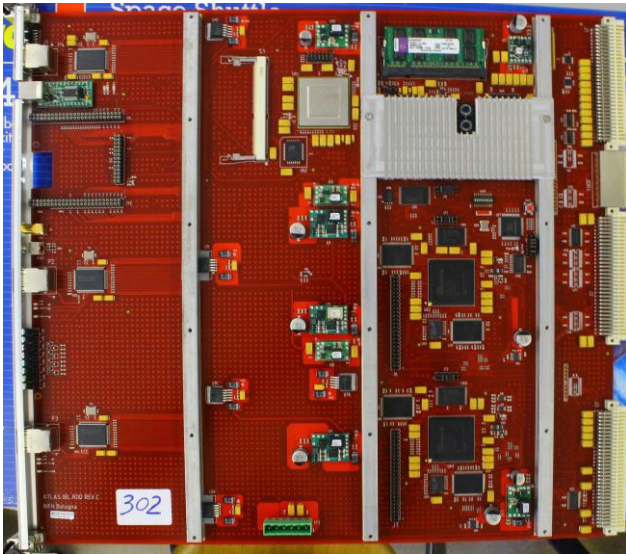


Fig. 7. ATLAS IBL ROD printed circuit board. This picture shows two Spartan6 FPGAs which are used as Slaves, one Texas Instruments DSP, VME connector, and one Spartan6 FPGA which is used as PRM. The Virtex5 FPGA is covered by heat sink near the DDR2-SODIMM module.

The two Xilinx Spartan6-LX150 are used for data gathering, event fragment building, and histogramming [8]. These FPGAs are called Slaves (The North Slave and South Slave). Each FPGA has 2GB DDR2-SDRAM modules and two 1Mx36 SSRAM modules to store histogram and calibration data. One Xilinx Virtex5-FX70T implements the heart of IBL ROD thus it is called as Master. This FPGA is dedicated as ROD controller and hosts a PowerPC which is in charge of system controls and non-real-time functions. Another one Xilinx Spartan6-LX45 FPGA is used as Program Reset Manager (PRM). The block diagram of IBL ROD is shown in figure 7.

## VI. SYSTEM INTEGRATION

The FE-I4 Front-end chip, The IBL ROD, and The IBL BOC are the main building block of IBL data acquisition system. The whole IBL data acquisition system requires 14 IBL BOC and IBL ROD pairs hosted in a single VME crate where a Timing Interface Modules (TIM) board distributes trigger information to all board [7]. Each BOC-ROD pair is able to handle data which is sent by 16 IBL modules. Recall that each IBL modules consist of 2 FE-I4 front-end chips. The total input bandwidth for each BOC-ROD pair is 5.12 Gb/s [7]. The data which is sent by IBL modules is received by IBL BOC via the RX optical modules then the BOC forward the data to the ROD after performing some data encoding. The ROD will further process the data. The integration diagram is shown in figure 9.

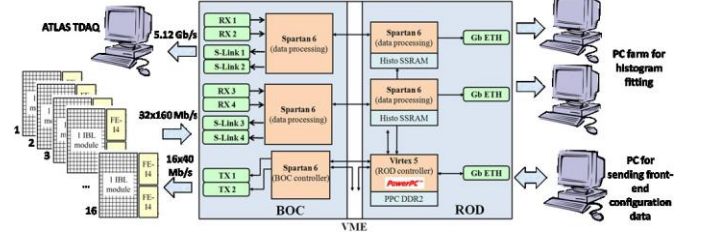


Fig. 9. The integration between IBL modules (the FE-I4 front-end chips), the IBL BOC, and the IBL ROD as the main building block of the whole IBL data acquisition system. [7]



Fig. 10. The IBL BOC (left) and the IBL ROD which are plugged in on VME Crate. The IBL ROD is connected back-to-back by the IBL BOC via the VME interface.

## VII. LOW-LEVEL SYSTEM TEST

The whole IBL data acquisition system will undergo some extensive test before they get finalization to be used in experiments. Because of the large size and a lot of components or module, the test itself can be cumbersome. Therefore we need to find out if there is a new method to test the whole system as well as each modules in an effective and efficient way. In this report, there are several test that have been done. They are the

| ROD ID | Test Date | Location | Program Reset Manager PRM (atl-git5/build/.mcs) | Master Ethernet / Virtex5-PowerPC (FW v6) | North Slave Ethernet / Spartan6 (FW v6) | South Slave Ethernet / Spartan6 (FW v6) | BOC IP Address (FW v6) | BOC2ROD North Slave | BOC2ROD South Slave | Clock (from BOC) | Remarks                                                                                                                                                                                                                           |
|--------|-----------|----------|-------------------------------------------------|-------------------------------------------|-----------------------------------------|-----------------------------------------|------------------------|---------------------|---------------------|------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 299    | 24-Jul-14 | SR-1     | OK                                              | OK                                        | Not Tested                              | Not Tested                              | 192.168.0.71           | OK                  | OK                  | OK               | BOC2ROD only tested AA-55 Pattern                                                                                                                                                                                                 |
| 294    | 25-Jul-14 | SR-1     | OK                                              | OK                                        | OK                                      | OK                                      | 192.168.0.42           | OK                  | OK                  | OK               | BOC2ROD with AA-55 and Counter Pattern                                                                                                                                                                                            |
| 303    | 25-Jul-14 | SR-1     | OK                                              | OK                                        | OK                                      | OK                                      | 192.168.0.42           | OK                  | OK                  | OK               | BOC2ROD with AA-55 and Counter Pattern                                                                                                                                                                                            |
| 298    | 12-Aug-14 | SR-1     | OK                                              | OK                                        | OK                                      | OK                                      | 192.168.0.42           | OK                  | OK                  | OK               | BOC2ROD with AA-55 and Counter Pattern<br>Sometimes during the test of Counter Pattern, the check_ok_a, check_ok_b, check_ok_c, and check_ok_d signal are logic low although we have power cycled, reflashed, and rerun the test. |
| 295    | 25-Jul-14 | SR-1     | OK                                              | OK                                        | OK                                      | OK                                      | 192.168.0.42           | OK                  | OK                  | OK               | BOC2ROD with AA-55 and Counter Pattern<br>Plastic shielding of VME Connector Receptacle is damaged.<br>Missing top lock hatch to lock it securely<br>Test is halted.                                                              |
| 297    | 24-Jul-14 | SR-1     | Not Tested                                      | Not Tested                                | Not Tested                              | Not Tested                              | Unknown                | Not Tested          | Not Tested          | OK               | The test have not been completed                                                                                                                                                                                                  |
| 301    | 12-Aug-14 | SR-1     | No Card                                         | OK                                        | OK                                      | OK                                      | 192.168.0.42           | OK                  | OK                  | OK               | BOC2ROD with AA-55 and Counter Pattern<br>Sometimes during the test of Counter Pattern, the check_ok_a, check_ok_b, check_ok_c, and check_ok_d signal are logic low although we have power cycled, reflashed, and rerun the test. |
| 293    | 24-Jul-14 | SR-1     | OK                                              | OK                                        | Not Tested                              | Not Tested                              | 192.168.0.71           | OK                  | OK                  | OK               | BOC2ROD only tested AA-55 Pattern                                                                                                                                                                                                 |
| 296    | 25-Jul-14 | SR-1     | OK                                              | OK                                        | OK                                      | OK                                      | 192.168.0.42           | OK                  | OK                  | OK               | BOC2ROD with AA-55 and Counter Pattern                                                                                                                                                                                            |
| 302    | No Card   | No Card  | No Card                                         | No Card                                   | Not Tested                              | Not Tested                              | ?                      | No Card             | No Card             | No Card          | No Card                                                                                                                                                                                                                           |
| 289    | 24-Jul-14 | SR-1     | OK                                              | OK                                        | Not Tested                              | Not Tested                              | 192.168.0.71           | OK                  | OK                  | OK               | BOC2ROD only tested AA-55 Pattern                                                                                                                                                                                                 |
| 290    | 25-Jul-14 | SR-1     | OK                                              | OK                                        | OK                                      | OK                                      | 192.168.0.42           | OK                  | OK                  | OK               | BOC2ROD with AA-55 and Counter Pattern                                                                                                                                                                                            |
| 291    | 24-Jul-14 | SR-1     | OK                                              | OK                                        | Not Tested                              | Not Tested                              | 192.168.0.71           | OK                  | OK                  | OK               | BOC2ROD only tested AA-55 Pattern                                                                                                                                                                                                 |
| 302    | 7-Aug-14  | PixelLab | OK                                              | OK                                        | OK                                      | OK                                      | 192.168.0.40           | OK                  | OK                  | OK               | BOC2ROD with AA-55 and Counter Pattern                                                                                                                                                                                            |
| 2      | 7-Aug-14  | PixelLab | OK                                              | OK                                        | OK                                      | OK                                      | 192.168.0.40           | OK                  | OK                  | OK               | BOC2ROD with AA-55 and Counter Pattern                                                                                                                                                                                            |
| 300    | No Card   | No Card  | No Card                                         | No Card                                   | Not Tested                              | Not Tested                              | ?                      | No Card             | No Card             | No Card          | No Card                                                                                                                                                                                                                           |
| 292    | 12-Aug-14 | SR-1     | OK                                              | OK                                        | OK                                      | OK                                      | 192.168.0.42           | OK                  | OK                  | OK               | BOC2ROD with AA-55 and Counter Pattern                                                                                                                                                                                            |
| 198    | 12-Aug-14 | SR-1     | OK                                              | OK                                        | OK                                      | OK                                      | 192.168.0.42           | OK                  | OK                  | OK               | BOC2ROD with AA-55 and Counter Pattern                                                                                                                                                                                            |

Fig. 11. Test Result for several test of IBL ROD and IBL BOC which are done in this report.

test for clock generator and clock mode at IBL ROD, the IBL ROD Master Ethernet Communication System, the IBL Slave Ethernet Communication System, the BOC-to-ROD communication tests, and the Program Reset Manager tests. Actually, there are several other tests that must be done such as S-Link communication test and DDR2 memory read and write test.

#### A. The IBL ROD Master Ethernet and Slaves Ethernet Communication Tests

There are three Ethernet ports in IBL ROD modules. One Ethernet port is dedicated to the IBL ROD Master which is implemented by using the Xilinx Virtex5 FPGA. The two Ethernet ports are dedicated to the IBL ROD Slaves. Each IBL ROD slave has one Ethernet connection. The test is started by first flash all of three FPGAs (the one Master and two Slave) using the appropriate compiled VHDL design files. To flash the FPGAs, JTAG chain is used.

After the FPGAs programmed successfully, we can proceed to the next step. We load the .ELF files to be executed at PowerPC processor in IBL ROD Master using Xilinx XMD Microprocessor Debugger. After the PowerPC processor is running, we can start the Ethernet Test for the Master by using packet analyzer software such as WireShark. The IP Address of the Master Ethernet depends on VME slot position on VME Crate.

The same method also applied for Slaves Ethernet test. After the FPGAs programmed successfully, we load the appropriate .ELF files to be executed at MicroBlaze processor in IBL ROD Slave using Xilinx XMD. One thing to remember is, the IP Address is configured within the .ELF files. After the program is running, we can easily test the Slave Ethernet by using packet analyzer software such as WireShark. Remember to give each slaves different IP Address thus different .ELF files.

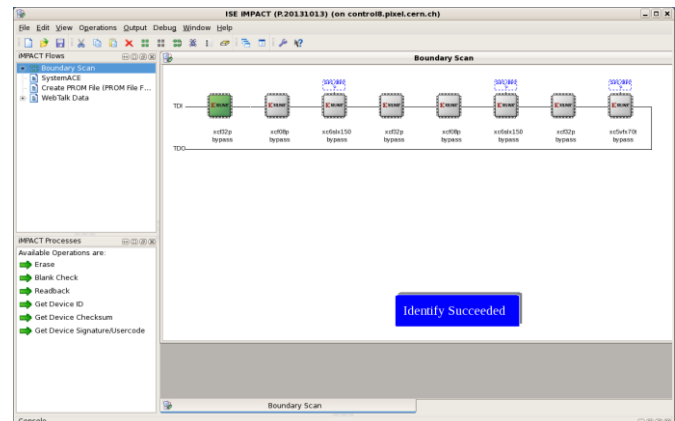


Fig. 12. JTAG Chain of the IBL ROD FPGAs which can be used to program all of the FPGAs.

```

Connected to "mb" target. id = 0
Starting GDB server for "mb" target (id = 0) at TCP port no 1234
XMD% dow /home/mbindi/ETHERNETTEST_BIS/105_00.elf
Downloading Program -- /home/mbindi/ETHERNETTEST_BIS/105_00.elf
section, .vectors.reset: 0x00000000-0x00000007
section, .vectors.sw.exception: 0x00000008-0x0000000f
section, .vectors.interrupt: 0x00000010-0x00000017
section, .vectors.hw.exception: 0x00000020-0x00000027
section, .text: 0xc0000000-0xc001f553
section, .init: 0xc001f554-0xc001f597
section, .fini: 0xc001f598-0xc001f5b7
section, .ctors: 0xc001f5b8-0xc001f5bf
section, .dtors: 0xc001f5c0-0xc001f5c7
section, .rodata: 0xc001f5c8-0xc0020713
section, .sdata2: 0xc0020714-0xc0020717
section, .data: 0xc0020718-0xc0020dab
section, .eh_frame: 0xc0020dac-0xc0020daf
section, .jcr: 0xc0020db0-0xc0020db3
section, .sdata: 0xc0020db4-0xc0020db7
section, .bss: 0xc0020db8-0xc00bba8f
section, .heap: 0xc00bba90-0xc00c5a8f
section, .stack: 0xc00c5a90-0xc00cfa8f
Download Progress...10.20.30.40.50.60.70.80.90..Done
Setting PC with Program Start Address 0x00000000
System Reset .... DONE

XMD% connect mb mdm -debugdevice devicnr 6 -cable type xilinx_platformusb

JTAG chain configuration
-----
Device ID Code IR Length Part Name
1 d5059093 16 XC32P
2 d5057093 16 XCF8P
3 44010093 6 XC6SLX150
4 d5059093 16 XC32P
5 d5057093 16 XCF8P
6 44010093 6 XC6SLX150
7 d5059093 16 XC32P
8 632c6093 10 XC5VFXT0T

```

MicroBlaze Processor Configuration :

Fig. 13. The Xilinx Microprocessor Debugger (XMD) to load .ELF files to PowerPC or MicroBlaze soft processor and analyze its execution step.



## B. The IBL ROD and IBL BOC Communication Tests

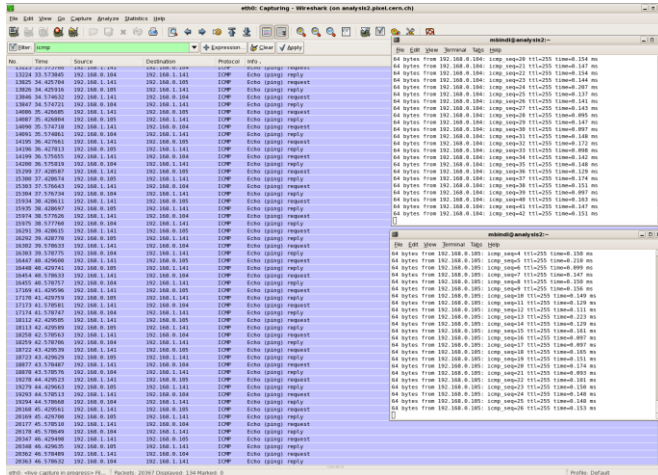


Fig. 14. WireShark is capturing ICMP packets that is sent by computer and returned back by IBL ROD in order to test the functionality of IBL ROD Ethernet port.

The IBL ROD and IBL BOC Communication Tests is somehow more complex than the previous test. We need to generate data on the BOC side and send the data into the ROD. Then, we analyze the data received by ROD using ChipScope. There are two pattern of data that are used in this test. The first one is the 0x55 – 0xAA pattern which repeat itself until the test is ended. This pattern will detect bit flips that might be occurred during the test. The other test pattern is the Counter pattern in which the data is increasing from 0x01, 0x02, 0x03, and so on. This Counter pattern will be used to detect any byte lost which can occur during test. For this test, we need ROD and BOC pair which are plugged in properly in VME crate. The ROD is configured to use the clock from the BOC.

The first step is almost the same. We have to program all of FPGAs on the IBL ROD using compiled VHDL Design files. Then, we open the ChipScope and wait until the ChipScope recognizes the JTAG Chain. We have to upload the same .BIT Files to both of IBL ROD Slaves. Then, we configured the ChipScope to display appropriate signal that we have interest to analyze it. Set the ChipScope to wait for trigger. The third step, we generate the data packets in BOC and send them to the ROD. Then, we can see the data that is received by the ROD in ChipScope.

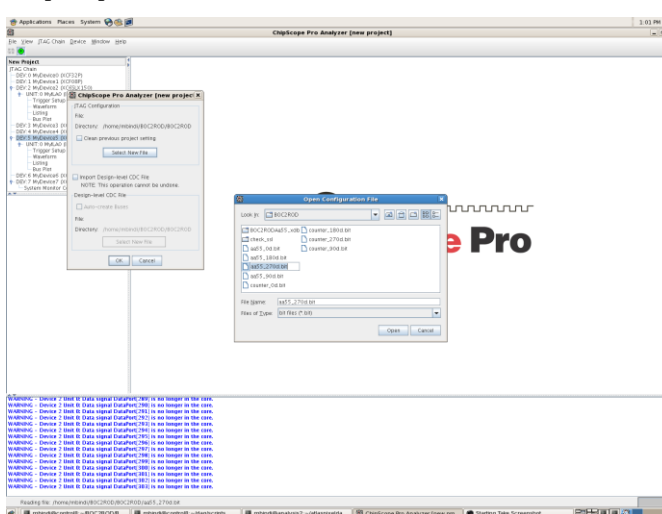


Fig. 15. Load the .BIT files to both of IBL ROD slaves using ChipScope Pro.

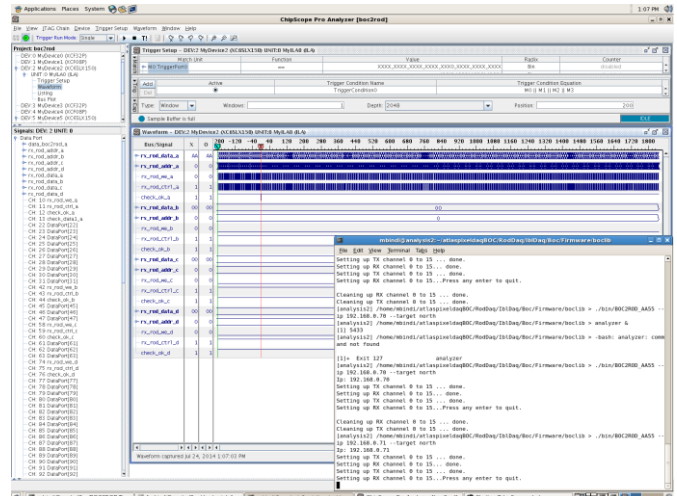


Fig. 16. Send a command to the IBL BOC to generate predefined data pattern and see the received data in the IBL ROD by using ChipScope.

This kind of test is really cumbersome because we need to scroll entire signal timeline to check the data that is received by IBL ROD whether the data is correct or not. This inefficient way of test must be improved by developing an automatic method that can tell us if there is any error during the test without looking the received data one by one. This test must be repeated for both IBL ROD Slave (the north slave and the south slave).

There is known bug in this test. After we give command to the IBL BOC to generate data pattern and terminate the command, the IBL ROD need to be reset in order to restart the test. If not, sometimes the IBL ROD doesn't respond to the data that is sent by IBL BOC.

## C. The IBL ROD Clock Test

The clock source of IBL ROD can be easily configured using the switch (number 6 switch) near the Lattice Oscillator. There are two ways of IBL ROD to get the clock. First, by using onboard Lattice Oscillator. This clock source can be used if there is no IBL BOC in pair. In other words, the IBL ROD is being used in standalone mode. The second way is to use clock which is supplied by the IBL BOC. This, of course, requires the IBL ROD and IBL BOC pair.

We can test the clock source for the IBL ROD by executing simple command in both PowerPC processor (IBL ROD Master) and the MicroBlaze processor (IBL ROD Slave). If the processor can run smoothly, then the IBL ROD has the properly configured clock source. Other way to check is by using visual inspection of LED indicator in the IBL ROD which indicates whether the IBL ROD gets the clock or not.

## D. The IBL ROD Program Reset Manager Test

The Program Reset Manager is implemented on the small Spartan6 FPGA in IBL ROD. To verify and reprogram this FPGA, we can use Xilinx IMPACT. First thing that we must change is the JTAG configuration cable. It doesn't use the same cable configuration as the previous tests. There will be a different JTAG configuration to flash PRM. After we flash the FPGA, we can easily verify the flashed program checksum using Xilinx IMPACT to make sure that PRM has been flashed correctly.

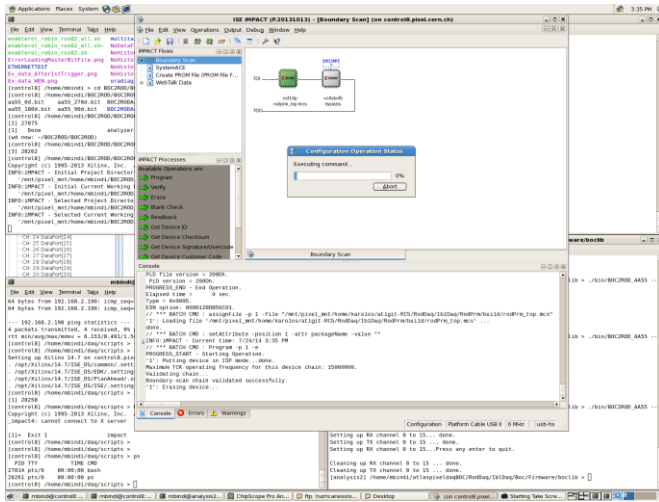


Fig. 17. Flashing and verifying the Program Reset Manager using Xilinx ISE IMPACT software.

### VIII. FUTURE IMPROVEMENT

As we can see from the test that we have done, a lot of efforts and time was spent to test each of the functionality of IBL Data Acquisition System. Some of the test even also requires the experience to operate advanced analysis program such as ChipScope which not every end-user can operate them easily. Moreover, there are still a lot of test that must be done and a lot of IBL ROD and IBL BOC pair to be tested. We have to develop an efficient and effective way to test the IBL ROD, IBL BOC and anything in between.

The proposed improvement for the test method of IBL Data Acquisition System is by adding some modules into VHDL Design Files to handle the test so that end-user doesn't need to reprogram the FPGAs to conduct specific test. On the other hand, we can build a Graphical User Interface software that can be used easily for the end user to test the IBL Data Acquisition System. The Graphical User Interface will send a command to the IBL ROD and IBL BOC to conduct specific test and display the result to the end-user. To achieve this functionality, we have to add some new block module to existing design and also build a software that can be run on computer to test the IBL Data Acquisition System.

#### A. Modifying the Design File and Firmware

We can avoid to flash the FPGAs using special design file to conduct a specific test by integrating all of the available test in one test module. This test module will responsible to handle the test command sent by user, executing appropriate tests, gathering the result, generating test scenario and test data, and send back the result to the user. This module will consume available logic block in FPGAs but it is very worth it to see its advantages. This test module will have its own register for the testing purpose as well as its ability to communicate with host PC via Ethernet interface.

#### B. Developing Graphical User Interface Software

The Graphical User Interface Software is a gate that bridges end-user to the IBL Data Acquisition System so that end-user can conduct several test and see the result easily without the need to operate some of advanced software. This Graphical

User Interface can send a command to the IBL ROD and IBL BOC to ask them to execute appropriate test. The command can be sent via Ethernet interface using TCP/UDP protocol. But, we must know the IP Address of the IBL ROD and IBL BOC that we want to test.

There are two proposed scenario in developing the graphical user interface. The first one is to build the graphical user interface to be executed in local computer. This is the simplest one but it will face a problem when end-user has different platform (i.e. operating system). The second one is to build a server that hosts the software to control the test. Then, end-users simply open their web browser to connect to the server. The web-based Graphical User Interface then can be used by end-users to do a test and see the result. The second idea is much more platform independent.

### IX. CONCLUSION

The ATLAS IBL Data Acquisition System is one of the most sophisticated data acquisition system ever built. It uses custom-designed electronics system to fulfill the requirements in ATLAS IBL upgrade. The preparation of this new system is now entering test phase where the data acquisition system is being tested and improved if there is some bug discovered during the test.

The test itself is somewhat time consuming and requires experience to use the advanced software. Therefore, we need to build an automatic test system which integrates a test modules, the modules that handles all of the test scenario, to the design of the data acquisition system. The end-user can conduct the test easily by using Graphical User Interface software which communicates with the test modules to execute and acquire test result.

### REFERENCES

- [1] Alessandro La Rosa on behalf of the ATLAS Collaboration. *ATLAS IBL: a challenging first step for ATLAS Upgrade at the LHC*.
- [2] Mario P. Giordani on behalf of the ATLAS Collaboration. *Overview of the ATLAS Insertable B-Layer (IBL) Project* on 36<sup>th</sup> International Conference of High Energy Physics 2012.
- [3] F. Djama on behalf of the ATLAS Collaboration. *Overview of the ATLAS Insertable B-Layer (IBL) Project*.
- [4] Marlon Barbero, David Arutinov, et. al. *The FE-I4 Pixel Readout Chip and the IBL Module* on Proceedings of Science.
- [5] FE-I4 Collaboration. *The FE-I4A Integrated Circuit Guide Version 11.6* June 21, 2011.
- [6] M. Wensing, B. Bergenthal, et. al. *IBL BOC Design and Firmware Manual* published on May 23<sup>rd</sup>, 2014.
- [7] Gabriele Balbi, Davide Falchieri, et. al. *IBL ROD Board Rev. C Reference Manual* published on November 2012.
- [8] Alessandro Polini, Graziano Bruni, et. al. *Design of the ATLAS IBL Readout System* on Technology and Instrumentation for Particle Physics 2011.

**Bagus Hanindhito** was born in Yogyakarta, Indonesia, in 1992. He is an electrical engineering undergraduate student at Department of Electrical Engineering, School of Electrical Engineering and Informatics, Institut Teknologi Bandung. In 2012 and 2014, he got the university awards as the most outstanding student in his faculty. He also got an opportunity to present his invention in biometrics security system at Fujitsu, Japan in 2013,

During his 2014 summer holiday, he joined CERN Summer Student Programme and he got an opportunity to join ATLAS Collaboration and did some tests on ATLAS IBL Data Acquisition System.

